WHAT IS CLAIMED IS:

1. A method for tri-state signal communication, comprising:

providing a first data signal;

providing a second data signal;

driving a data line to a first state if the first data signal is a logic zero;

releasing the data line to a second state if the first data signal is a logic one; and

driving the released data line to a third state if the first data signal is a logic one and the second data signal is a logic one.

2. The method of Claim 1, wherein the data line is coupled to a first voltage level using a pull-up resistor, and driving a data line to a first state comprises pulling the voltage of data line from the first voltage level towards a zero voltage level.

3. The method of Claim 1, wherein releasing the data line to a second state comprises placing an output of an amplifier coupled to the data line into an open drain state.

4. The method of Claim 1, wherein driving the released data line to a third state comprises:

placing an output of a first amplifier coupled to the data line into an open drain state; and

driving a second amplifier coupled to the data line.

5. The method of Claim 1, wherein the data line is coupled to a first voltage level using a pull-up resistor, and driving the released data line to a third state comprises:

placing an output of a first amplifier coupled to the data line into an open drain state; and

driving a second amplifier coupled to the data line to transition the voltage of the data line from the first voltage level to a second voltage level representing the third state.

6. The method of Claim 1, wherein:

the first amplifier comprises an open drain Gunning Transceiver Logic (GTL) buffer; and

the second amplifier comprises a Stub Series Terminated Logic (SSTL) output driver.

7. The method of Claim 1, wherein:

the first state comprises an approximate 0.4 voltage level on the data line;

the second state comprises an approximate 1.2 voltage level on the data line; and

the third state comprises an approximate 2.3 voltage level on the data line.

8. A tri-state transmitter comprising:

a first amplifier operable to receive a first data signal, the first amplifier operable to drive a data line to a first state if the first data signal is a logic zero, the first amplifier further operable to release the data line to a second state if the first data signal is a logic one; and

a second amplifier operable to receive a second data signal, the second amplifier operable to drive the released data line to a third state if the first data signal is a logic one and the second data signal is a logic one.

9. The tri-state transmitter of Claim 8, further comprising a pull-up resistor coupling the data line to a first voltage level, wherein the first amplifier drives the data line to the first state by pulling the voltage of the data line from the first voltage level towards a zero voltage level.

10. The tri-state transmitter of Claim 8, wherein the first amplifier establishes an open drain state on its output to release the data line to the second state.

11. The tri-state transmitter of Claim 8, wherein the first amplifier establishes an open drain state to release the data line so that the second amplifier can drive the data line to the third state.

12. The tri-state transmitter of Claim 8, further comprising a pull-up resistor coupling the data line to a first voltage level, wherein the first amplifier establishes an open drain state to release the data line so that the second amplifier can drive the data line to a third state represented by a second voltage level, the first voltage level being between the second voltage level and a zero voltage level.

13. The tri-state transmitter of Claim 8, wherein:

the first amplifier comprises an open drain Gunning Transceiver Logic (GTL) buffer; and

the second amplifier comprises a Stub Series Terminated Logic (SSTL) output driver.

14. The tri-state transmitter of Claim 8, wherein:

the first state comprises an approximate 0.4 voltage level on the data line;

the second state comprises an approximate 1.2 voltage level on the data line; and

the third state comprises an approximate 2.3 voltage level on the data line.

15. An apparatus for tri-state signal communication, comprising:

means for providing a first data signal;

means for providing a second data signal;

means for driving a data line to a first state if the first data signal is a logic zero;

means for releasing the data line to a second state if the first data signal is a logic one; and

means for driving the released data line to a third state if the first data signal is a logic one and the second data signal is a logic one.

16. The apparatus of Claim 15, wherein the data line is coupled to a first voltage level using a pull-up resistor, and means for driving the released data line to a third state comprises:

means for placing an output of a first amplifier coupled to the data line into an open drain state; and

means for driving a second amplifier coupled to the data line to transition the voltage of the data line from the first voltage level to a second voltage level representing the third state.

17. The apparatus of Claim 15, wherein:

the means for driving a data line comprises an open drain Gunning Transceiver Logic (GTL) buffer; and

the means for driving the released data line comprises a Stub Series Terminated Logic (SSTL) output driver.

18. The apparatus of Claim 15, wherein:

the first state comprises an approximate 0.4 voltage level on the data line;

the second state comprises an approximate 1.2 voltage level on the data line; and

the third state comprises an approximate 2.3 voltage level on the data line.

19. A communication server comprising:

a network interface operable to communicate with a data network;

at least one linecard coupled to the network interface, the linecard operable to couple to customer premises equipment to deliver data services to the customers; and

a bus coupling the network interface to the linecard, the bus comprising a plurality of tri-state transmitter/receiver pairs, each transmitter/receiver pair comprising:

a first amplifier operable to receive a first data signal, the first amplifier operable to drive a data line to a first state if the first data signal is a logic zero, the first amplifier further operable to release the data line to a second state if the first data signal is a logic one;

a second amplifier operable to receive a second data signal, the second amplifier operable to drive the released data line to a third state if the first data signal is logic one and the second data signal is a logic one; and

a receiver operable to resolve voltages on the data line to determine if the data line is in the first state, the second state, or the third state.

20. The communication server of Claim 19, wherein the linecard supports XDSL communication with customer premises equipment.

21. The communication server of Claim 19, wherein the bus comprises:

a backplane;

a first physical interface that couples the network interface to the backplane; and

a second physical interface that couples the linecard to the backplane.